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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,052	01/28/2004	Harald Seidl	INF-130	9622
48154	7590	09/13/2005		
SLATER & MATSIL LLP 17950 PRESTON ROAD SUITE 1000 DALLAS, TX 75252			EXAMINER KENNEDY, JENNIFER M	
			ART UNIT 2812	PAPER NUMBER

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/765,052

Applicant(s)

SEIDL ET AL.

Examiner

Jennifer M. Kennedy

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 July 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

Response to Amendment

In view of Applicant's amendments to the claims, the objection of claim 3 has been withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, and 8-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schrems et al. (U.S. Patent No. 6,200, 873) in view of Klaus et al. ("Atomic Layer deposition of SiO₂ Using Catalyzed and Uncatalyzed Self-Limiting Surface Reactions", provided in IDS).

In re claim 1, Schrems et al. disclose a method for fabricating patterned ceramic layers on areas of a relief that are arranged essentially perpendicular to a substrate surface, comprising:

providing a semiconductor substrate (101);

forming relief structures (108 with 151) which are trench structures formed within a top side of the substrate, wherein internal areas are arranged essentially perpendicular to the top side of the substrate;

filling the relief structures with a resist (152) in physical contact with the trench in the substrate and subsequently isotropically etching the resist to remove the resist to a relief depth, wherein a resist layer is obtained (see column 4, line 55 through column 5, line 12, and column 18, lines 16-25);

depositing a ceramic layer synthesized from a ceramic material (see column 5, lines 12-40);

anisotropic etching of the ceramic layer, wherein the ceramic layer remains at the areas arranged perpendicular to the top side of the substrate, and wherein a top side of the resist layer situated below the ceramic layer is at least partially uncovered (see column 5, lines 40-50 and Figure 6b); and

subsequently removing the resist layer (see column 5, lines 50-65).

Schrems et al. does not disclose the method wherein the ceramic material is formed by means of a low temperature ALD method, wherein the low temperature ALD method is performed at a temperature lower than a softening temperature of the resist.

Klaus et al. disclose the method of forming a ceramic layer by means of a low temperature ALD method, wherein the low temperature ALD method is performed at a temperature lower than a softening temperature of the resist (see entire article,

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especially second paragraph of page 436, first paragraph of 437, the second and third full paragraph of 438).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a low temperature ALD method in the method of Schrems et al. in order to allow for a conformal layer within a high aspect ratio trench capacitor and because it allows the incorporation of polymers and other temperature sensitive materials that are useful in microelectronic devices (see second paragraph of page 436).

In re claim 8, Klaus et al. disclose the method wherein the ceramic layer is produced by a catalytic ALD method, wherein the semiconductor substrate is arranged in a reaction space, and a cycle is carried out, comprising:

introducing a first precursor compound into the reaction space, wherein the first precursor compound is adsorbed on the surface of the substrate;

removing excess unbound first precursor compound from the reaction space;

introducing a second precursor compound into the reaction space, wherein the second precursor compound is adsorbed on the surface of the substrate; and

removing unbound second precursor compound from the reaction space, wherein a catalyst is added to at least one precursor compound, wherein the catalyst catalyses the reaction of the first precursor compound with the second precursor compound (see entire article, especially page 436 and 438).

In re claim 9, Klaus et al. disclose the method wherein the catalyst is an aromatic nitrogen base (see entire article, especially page 436 and 438).

In re claim 10, Klaus et al. disclose the method wherein the aromatic nitrogen base is pyridine (see entire article, especially page 436 and 438).

In re claim 11, Schrems et al. and Klaus et al. disclose the method wherein the ceramic layer is synthesized from SiO_2 , Si_3N_4 , Al_2O_3 or a combination of these compounds (168 of Schrems and abstract of Klaus et al.).

In re claim 12, Schrems et al. disclose the method wherein filling the relief structures with a resist to a specific relief depth comprises:

filling the relief structure completely with the resist; and

removing the resist layer to the specific relief depth (see column 4, line 55 through column 5, line 12; and Figures 6a-6b).

In re claim 13, Schrems et al. disclose the method wherein the resist layer is planarized after the relief has been completely filled with the resist (see column 4, line 55 through column 5, line 12).

In re claim 14, Schrems et al. disclose the method wherein the relief structures comprise high aspect ratio trenches (see Figure 6a).

In re claim 15, Schrems et al. disclose the method wherein the trenches are functionally processed to produce capacitors (see Figure 6g and abstract).

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In re claim 16, Schrems et al. disclose a method for fabricating patterned ceramic layers on areas of a relief that are arranged essentially perpendicular to a substrate surface, comprising:

providing a semiconductor substrate (101);

forming relief structures (106 with 151) which are trench structures formed within a top side of the substrate (108), wherein internal areas are arranged essentially perpendicular to the top side of the substrate;

filling the relief structures with a resist (152) in physical contact with the trench in the substrate and subsequently isotropically etching the resist to remove the resist to a relief depth, wherein a resist layer is obtained (see column 4, line 55 through column 5, line 12, and column 18, lines 16-25); and

depositing a ceramic layer (168) synthesized from a ceramic material.

Schrems et al. does not disclose the method wherein the ceramic material is formed by means of a low temperature deposition method, wherein the low temperature deposition method is performed at a temperature lower than a softening temperature of the resist.

Klaus et al. disclose the method of forming a ceramic layer by means of a low temperature method, wherein the low temperature method is performed at a temperature lower than a softening temperature of the resist (see entire article, especially second paragraph of page 436, first paragraph of 437, the second and third full paragraph of 438).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a low temperature process in the method of Schrems et al. in order to allow for a conformal layer within a high aspect ratio trench capacitor and because the low temperature process allows the incorporation of polymers and other temperature sensitive materials that are useful in microelectronic devices (see second paragraph of page 436).

In re claim 17, Klaus et al. disclose the method wherein the low temperature deposition method comprises an ALD method (see entire article, especially second paragraph of page 436, first paragraph of 437, the second and third full paragraph of 438).

In re claim 18, Klaus et al. disclose the method wherein the deposition of the ceramic layer is carried out at a temperature of less than 100 °C (see entire article, especially the second and third full paragraph of 438).

In re claim 19, Schrems et al. disclose the method wherein a heat treatment step for densifying the ceramic layer is carried out after the removal of the resist layer (see column 5, lines 12-40).

In re claim 20, Schrems et al. disclose a method for fabricating patterned ceramic layers on areas of a relief structure formed within a substrate, comprising:
providing a semiconductor substrate (101);

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forming relief structures (108 with 151) which are trench structures within a top side of the substrate;

filling the relief structures with a resist (152) in physical contact with the trench structures in the substrate and subsequently isotropically etching the resist to a relief depth, wherein a resist layer is obtained (see column 4, line 55 through column 5, line 12, and column 18, lines 16-25);

depositing a ceramic layer synthesized from a ceramic material (see column 5, lines 12-40);

anisotropic etching of the ceramic layer, wherein the ceramic layer remains at the areas arranged perpendicular to the top side of the substrate, and wherein a top side of the resist layer situated below the ceramic layer is at least partially uncovered (see column 5, lines 40-50 and Figure 6b); and

removing the resist layer (see column 5, lines 50-65).

Schrems et al. does not disclose the method wherein the ceramic material is formed by means of a low temperature ALD method, wherein the low temperature ALD method is performed at a temperature lower than a softening temperature of the resist.

Klaus et al. disclose the method of forming a ceramic layer by means of a low temperature ALD method, wherein the low temperature ALD method is performed at a temperature lower than a softening temperature of the resist (see entire article, especially second paragraph of page 436, first paragraph of 437, the second and third full paragraph of 438).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a low temperature ALD method in the method of Schrems et al. in order to allow for a conformal layer within a high aspect ratio trench capacitor and because it allows the incorporation of polymers and other temperature sensitive materials that are useful in microelectronic devices (see second paragraph of page 436).

Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schrems et al. (U.S. Patent No. 6,200, 873) and Klaus et al. ("Atomic Layer deposition of SiO₂ Using Catalyzed and Uncatalyzed Self-Limiting Surface Reactions", provided in IDS) in view of Nguyen (U.S. Patent No. 6,689,220).

The combined Schrems et al. and Klaus et al. disclose the method as claimed and rejected above, including method wherein the ceramic layer is deposited by an ALD method, in which the semiconductor substrate is arranged in a reaction space and a cycle is carried out, comprising:

introducing a first precursor compound into a reaction space, wherein the first precursor compound is adsorbed on the surface of the substrate;

removing unbound first precursor compound from the reaction space;

introducing a second precursor compound into the reaction space, wherein the second precursor compound is adsorbed on the surface of the substrate; and

removing unbound second precursor compound from the reaction space (see Klaus et al., entire article, especially page 436, and third full paragraph of 438).

Schrems et al. and Klaus et al. do not disclose the method wherein the ALD method is a radical-assisted ALD method.

Nguyen disclose the method of utilizing a radical-assisted ALD method (see column 2, lines 23-42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a radical assisted ALD method in order to allow for lower temperature processing and to allow for wider selection of precursor solutions.

In re claim 3, the combined Schrems et al., Klaus et al. and Nguyen disclose the method wherein radicals are produced from at least one portion of a first or a second precursor compound, wherein the radicals react with the precursor compound adsorbed on the substrate surface to form the deposited material (see Nguyen, column 7, line 50 through column 8, line 63).

In re claim 4, the combined Schrems et al., Klaus et al. and Nguyen disclose the method wherein the cycle is repeated until a desired layer thickness of the ceramic layer is reached (see Klaus et al. page 436, second to last paragraph or Nguyen column 3, lines 60-65).

In re claim 5, the combined Schrems et al., Klaus et al. and Nguyen disclose the method wherein the radicals are produced by means of a plasma (see Nguyen see column 7, lines 20-30).

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In re claim 6, the combined Schrems et al., Klaus et al. and Nguyen disclose the method wherein the precursor compound is deposited in a cycle, comprising the following steps:

introducing the precursor compound into the reaction space and removing unbound precursor compound from the reaction space, wherein the cycle is repeated at least once (see Klaus et al. see entire article, especially second paragraph of page 436, first paragraph of 437, the second and third full paragraph of 438)..

producing radicals from at least one portion of the precursor compound, wherein the radicals react with the precursor compound deposited on the substrate surface (see column 7, line 50 through column 8, line 63).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schrems et al. (U.S. Patent No. 6,200, 873, hereinafter referred to as Schrems et al. '873), Klaus et al. ("Atomic Layer deposition of SiO_2 Using Catalyzed and Uncatalyzed Self-Limiting Surface Reactions", provided in IDS), and Nguyen (U.S. Patent No. 6,689,220) in view of Schrems (U.S. Patent No. 6,500,707, herein after referred to as "Schrems '707).

The combined Schrems et al. '873, Klaus et al. and Nguyen disclose the method as claimed and rejected above, but does not disclose the method wherein the ceramic layer is constructed from Al_2O_3 . Schrems '707 disclose the method of forming a dielectric of either silicon oxide or aluminum oxide (see column 9, lines 15-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the collar of Schrems et al. '873 with aluminum oxide, because as Schrems '707 discloses aluminum oxide and silicon oxide are interchangeable as trench dielectrics since they allow for electrical insulation and since it has been held that the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945). See also *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960). Further, the examiner notes that the method of Klaus et al. is suitable for aluminum oxide as well as silicon oxide (see Klaus et al. page 437, second full paragraph)

Response to Arguments

Applicant's arguments filed July 5, 2005 have been fully considered but they are not persuasive. Applicant argues that Schrems does not disclose the method of forming the resist in contact with the trench since Schrems teaches the method of lining the trench with a liner layer or layers. The examiner notes that while the liner (151) of Schrems may be lining the substrate, the liner defines another trench or relief structure within the substrate with a smaller diameter or opening. The Applicant has not required that the resist be physically in contact with the substrate sidewall, but only that a relief structure which are trench structures be formed within a top side of the substrate and that the resist be in physical contact the trench in the substrate. Thus, the trench (108) line with the liner (151) can be considered the trench or relief structure of the present

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claim limitation, which is provided in physical contact with the resist (152, see Figure 6a).

Applicant also argues that Schrems make the use of a resist for the sacrificial layer unworkable because the collar layer deposition at Col 17, lines 53-60 require temperatures in excess of 1000 degrees C. The examiner disagrees and notes that Schrems clearly discloses an embodiment in which the photoresist may be used instead of polysilicon (see column 18, lines 15-25). Therefore, Schrems et al. disclose that a resist would be workable in the method as disclosed, and Applicant's mere allegation of there being no possibility of success is not persuasive.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Jennifer M. Kennedy
Primary Examiner
Art Unit 2812

jmk